KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____ DATE: Dec. 15th ,2015

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

TX14D201MM2BAA

Contents

ACCEPTED BY: _____ PROPOSED BY: Oblack Tsai

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 5.7” QVGA of 4:3 format amorphous silicon TFT. The pixel format is stripe arrangement. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX14D201MM2BAA
Module Dimensions	131(W) mm x 104.2(H) mm x 7.8 (D) mm
LCD Active Area	115.2(W) mm x 86.4(H) mm
Pixel Pitch	0.36(W) mm x 0.36 (H) mm
Resolution	320 (W) x 240(H) Dots
LCD Type	Transmissive monochrome TFT; Normally White
Display Type	Active Matrix
Gray Scale	16
Backlight	Light Emitting Diode(LED)
Weight	120 g
Interface	8-bit parallel bi-directional interface with 8080 ; 40pins
Power Supply Voltage	3.3V for LCD; 12V for backlight
Power Consumption	0.069W for LCD; 1.32W for backlight
Viewing Direction	12 O’clock (without image inversion and least brightness change)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	5.5	V	-
Input Voltage of Logic	V_I	-0.3	V_{DD}+0.3	V	Note 1
Operating Temperature	Top	-30	80	°C	Note 2
Storage Temperature	Tst	-30	80	°C	Note 2

Note 1: The rating is defined for the signal voltages of the interface such as A0, CS, /WR, /RD and Data bus.

Note 2: The maximum rating is defined as above based on the panel chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

$T_a = 25\ ^{\circ}C,\ V_{SS} = 0V$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Input Voltage of Logic	V_I	"H" level	$0.7V_{DD}$	-	V_{DD}	V	Note 1
		"L" level	V_{SS}	-	$0.3V_{DD}$		
Power Supply Current	I_{DD}	V_{DD}-V_{SS} =3.3V	-	20	30	mA	Note 2,3
Frame Frequency	f_{Frame}	-	-	60	-	Hz	-

Note 1: The rating is defined for the signal voltages of the interface such as A0, CS, /WR, /RD, REST and data bus.

Note 2: An all black check pattern is used when measuring I_{DD}, f_{Frame} is set to 60 Hz. 0.5A fuse is applied in the module for I_{DD}. For display activation and protection purpose, power supply is recommended larger than 1.25A to start the display and break fuse once any short circuit occurred.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	Backlight Unit	11	12.0	13	V	Note 1
LED Forward Current	I_{LED}	0V;0%duty	-	110	135	mA	Note 2
		3.3VDC;100%duty	-	15	20		
LED Lifetime	-	I_{LED}=110mA	-	50K	-	hrs	Note 3

Note 1: As Fig. 5.1 shown, LED current is constant, 110 mA, controlled by the LED driver when applying 12V.

Note 2: Dimming function can be obtained by applying DC voltage or PWM signal from the display interface CN1. The recommended PWM signal is 1K ~ 10K Hz with 3.3V amplitude.

Note 3: The estimated lifetime is specified as the time to reduce 50% brightness by applying 110 mA at 25°C.

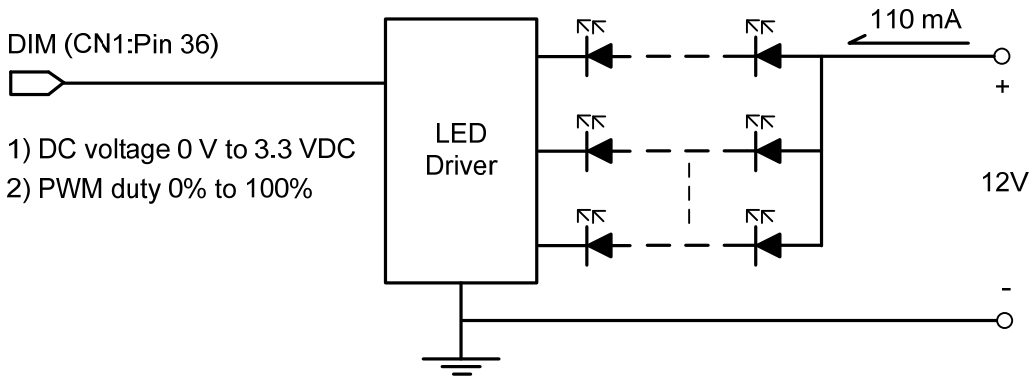


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\,^{\circ}C$, $f_{Frame} = 60\,Hz$, $V_{DD} = 3.3V$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	I_{LED}= 110mA $\phi = 0^{\circ}, \theta = 0^{\circ}$	1200	1500	-	cd/m^2	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2
Contrast Ratio		CR		600	1200	-	-	Note 3
Response Time		Tr + Tf	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	35	-	ms	Note 4
Viewing Angle		θ x	$\phi = 0^{\circ}$, CR ≥ 10	70	80	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}$, CR ≥ 10	70	80	-		
		θ y	$\phi = 90^{\circ}$, CR ≥ 10	70	80	-		
		θ y′	$\phi = 270^{\circ}$, CR ≥ 10	70	80	-		
Color Chromaticity	White	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	0.24	0.29	0.34		
		Y		0.24	0.29	0.34		

Note 1: The brightness is measured from the center point of the panel, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \text{ X100\%}$$

which is based on the brightness values of the 9 points in active area measured by BM-5 as shown in Fig. 6.2.

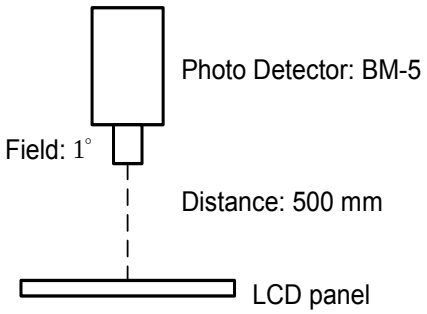


Fig 6.1

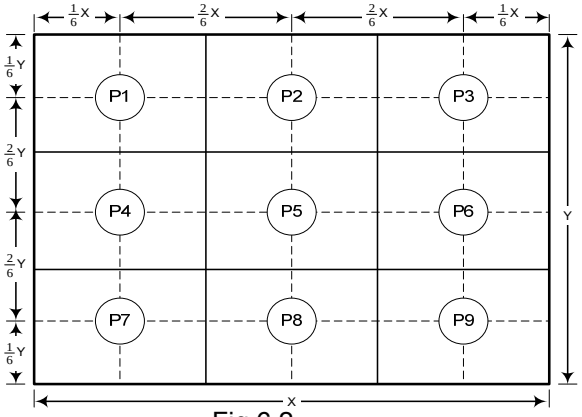


Fig 6.2

Note 3: The Contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 90% brightness to 10% brightness when the data is from white to black. Oppositely, Falling time is the period from 10% brightness rising to 90% brightness.

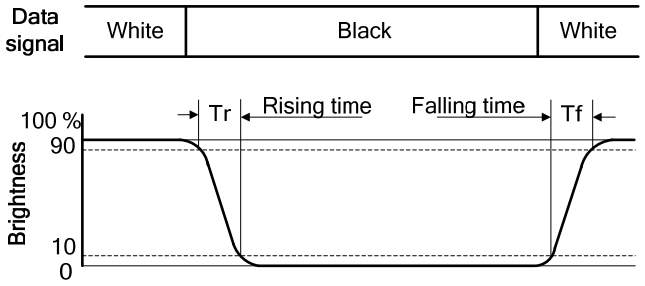


Fig 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

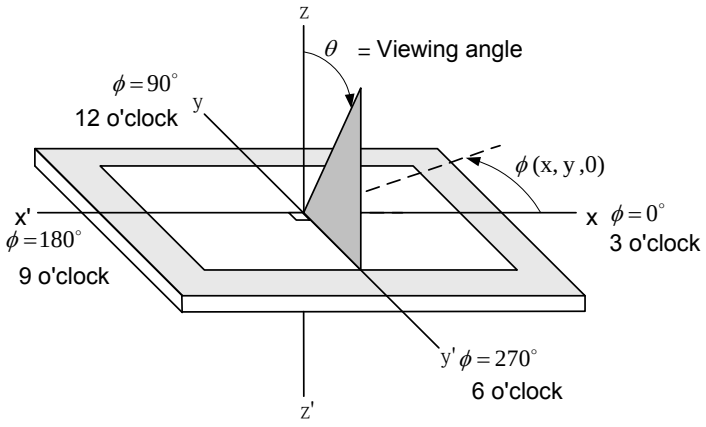
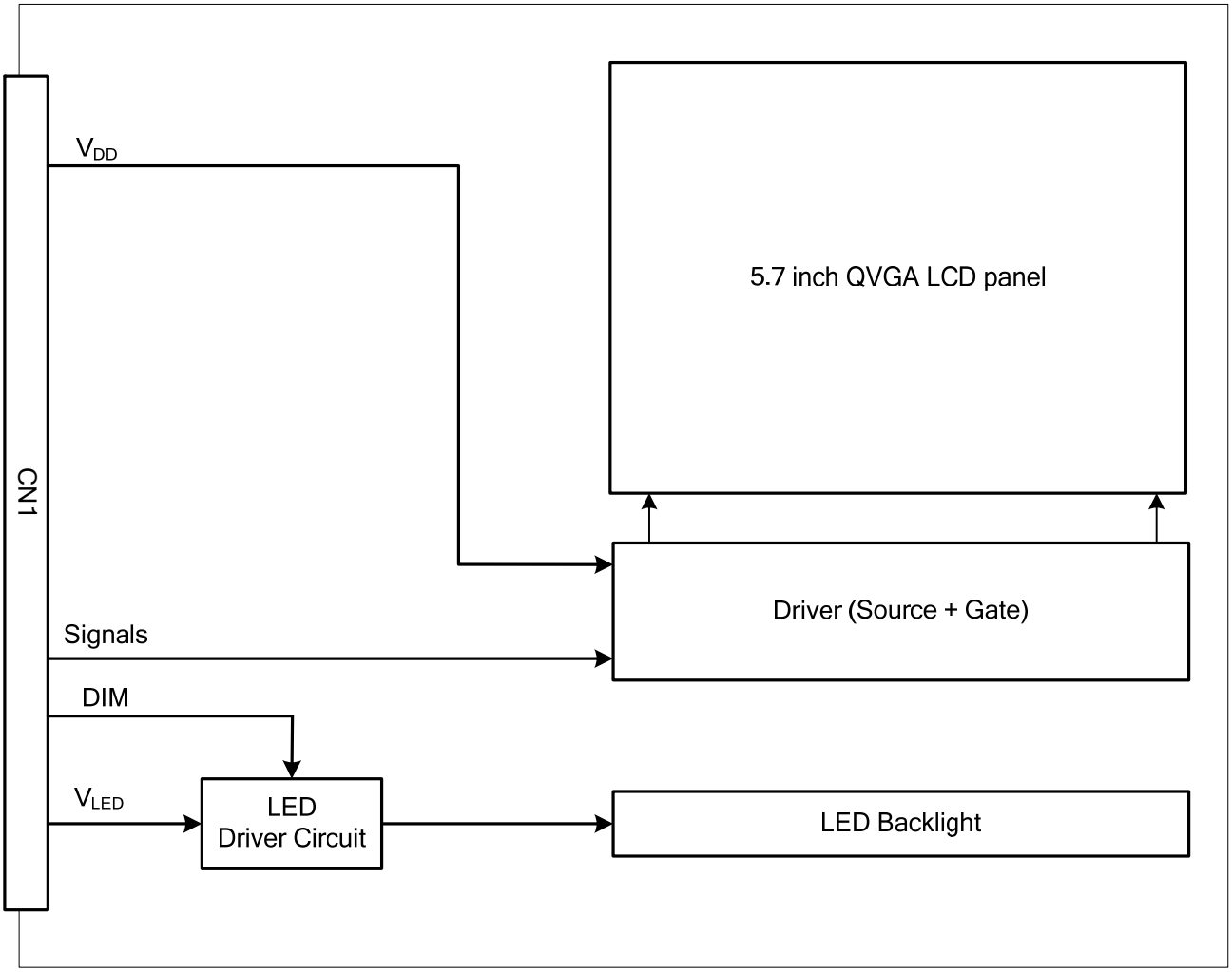


Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note 1: Signals are a A0, CS, /WR, /RD, RESET and data bus.

8. RELIABILITY TESTS

Test Item	Condition	
High Temperature	1) Operating 2) 80°C	240 hrs
Low Temperature	1) Operating 2) -30°C	240 hrs
High Temperature	1) Storage 2) 80°C	240 hrs
Low Temperature	1) Storage 2) -30°C	240 hrs
Heat Cycle	1) Operating 2) –20°C ~70°C 3) 3hrs~1hr~3hrs	240 hrs
Thermal Shock	1) Non-Operating 2) -35°C↔85°C 3) 0.5 hr↔0.5 hr	240 hrs
High Temperature & Humidity	1) Operating 2) 40°C& 85%RH 3) Without condensation	240 hrs (Note 3)
Vibration	1) Non-Operating 2) 20～200 Hz 3) 2G 4) X, Y, and Z directions	1 hr for each direction
Mechanical Shock	1) Non-Operating 2) 10 ms 3) 50G 4) ±X, ±Y and ±Z directions	Once for each direction
ESD	1) Operating 2) Tip: 150 pF, 330Ω 3) Air discharge for glass: ± 8KV 4) Contact discharge for metal frame: ± 8KV	1) Glass: 9 points 2) Metal frame: 8 points (Note 4)

Note 1: Display functionalities are inspected under the conditions defined in the specification after the reliability tests.

Note 2: The display is not guaranteed for use in corrosive gas environments.

Note 3: Under the condition of high temperature & humidity, if the temperature is higher than 40℃, the humidity needs to be reduced as Fig. 8.1 shown.

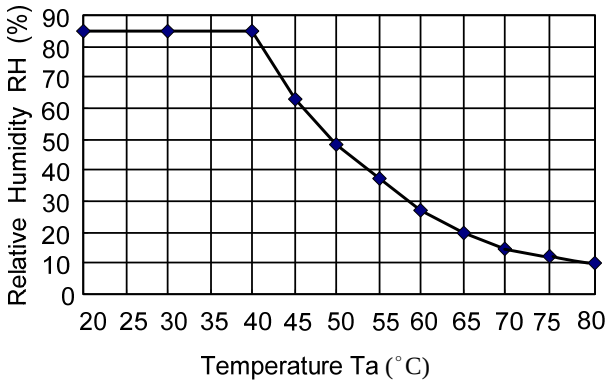


Fig. 8.1

Note 4: All pins of LCD interface (CN1) have been tested by ± 100V contact discharge of ESD under non-operating condition.

9. LCD INTERFACE

9.1 INTERFACE PIN CONNECTIONS

The display interface connector is FA5S040HP1R3000 made by JAE (Thickness: 0.3 ± 0.05mm; Pitch: 0.5 ± 0.05mm) and more details of the connector are shown in the section of outline dimension.

Pin assignment of LCD interface is as below:

Pin No.	Signal	Function	Pin No.	Signal	Function
1	V_{SS}	GND	21	NC	No Connection
2	V_{DD}	Power Supply for Logic	22		
3	V_{DD}		23		
4	A0	Command / Data identification pin	24		
5	/WR	Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal	25		
6	/RD	Read enable input pin. When /RD is “L”, D[7:0] are in output mode	26		
7	D0	Data bus	27		
8	D1		28		
9	D2		29		
10	D3		30		
11	D4		31		
12	D5		32		
13	D6		33		
14	D7		34	V_{SS}	GND
15	CSB	Chip select input pin. When CSB is non-active (CSB=’H’), D [7:0] pins are high impedance.	35		
16	RESET	Reset input pin. Active when it is ‘L’. This pin is effective when RSTEN pin is ‘H’.Initialization is executed when this pin is set to ‘L’. SWRESET command must be required after initialization.	36	DIM	Brightness dimming (Note 1)
17	NC	No Connection	37	V_{LED}	12VDC
18	NC		38		
19	V_{SS}	GND	39		
20	V_{SS}		40		

Note 1: Normal brightness: 0V or 0% PWM duty; Brightness control: 0V to 3.3V DC or 0% to 100% PWM duty.

9.2 FUNCTIONS

9.2.1 Parallel Interface

8080 series MCU		A0	CSB	Interface Transmission Type
/WR	/RD			
↑	H	L	L	Write Command
↑	H	H		Write Display Data or Parameter
H	↓	H		Read Display Data or Parameter Start
H	↑	H		Read Display Data or Parameter Stop

Note 1: Reading Display Data or Parameter is specified by the instruction before the read operation.

Note 2: When reading Display Data (DDRAM contents), the first output byte is dummy byte.

Note 3: When reading Parameter (temperature, status and PROM data), the first output byte is valid.

Command List

No	Command	Hex	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Parameter
1	NOP	00h	0	1	↑	0	0	0	0	0	0	0	0	No operation	00
			1	1	↑	1	0	1	0	0	1	0	1		A5
2	SWRESET	AEh	0	1	↑	1	0	1	0	1	1	1	0	Software reset	AE
			1	1	↑	1	0	1	0	0	1	0	1		A5
3	VCDAT	54h	0	1	↑	0	1	0	1	0	1	0	0	VCOM Offset Data	54
			1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0		0E
			1	1	↑	0	VcomD16	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10		00
			1	1	↑	0	VcomD26	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20		00
			1	1	↑	1	0	1	0	0	1	0	1		A5
4	PWRCTL	61h	0	1	↑	0	1	1	0	0	0	0	1	All Power Control	61
			1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON		8F
			1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0		04
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
5	EVSET1	62h	0	1	↑	0	1	1	0	0	0	1	0	Set VCOM / VGH / VGL	62
			1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0		14
			1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0		0B
			1	1	↑	0	0	0	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0		0B
			1	1	↑	1	0	1	0	0	1	0	1		A5

Command List

No	Command	Hex	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Parameter
6	DISSET2	33h	0	1	↑	0	0	1	1	0	0	1	1	Display Set2	33
			1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0		07
			1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0		2F
			1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0		10
			1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0		26
7	EVSET2	63h	0	1	↑	0	1	1	0	0	0	1	1	Set GVDD / GVCL	63
			1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0		0E
			1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0		0E
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
8	DISSET1	32h	0	1	↑	0	0	1	1	0	0	1	0	Display Set1	32
			1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0		32
			1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0		2A
			1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8		80
			1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0		2A
9	GAMSET4P1	91h	0	1	↑	1	0	0	1	0	0	0	1	Gamma Set 4bpp Positive1	91
			1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00		00
			1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10		13
			1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20		16
			1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30		18
10	GAMSET4P2	92h	0	1	↑	1	0	0	1	0	0	1	0	Gamma Set 4bpp Positive2	92
			1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40		19
			1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50		1A
			1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60		1B
			1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70		1D
11	GAMSET4P3	93h	0	1	↑	1	0	0	1	0	0	1	1	Gamma Set 4bpp Positive3	93
			1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80		1F
			1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90		20
			1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0		22
			1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0		24
12	GAMSET4P4	94h	0	1	↑	1	0	0	1	0	1	0	0	Gamma Set 4bpp Positive4	94
			1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0		26
			1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0		29
			1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0		2F
			1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0		3F
13	GAMSET4N1	99h	0	1	↑	1	0	0	1	1	0	0	1	Gamma Set 4bpp Positive4	99
			1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00		00
			1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10		13
			1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20		15
			1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30		17

Command List

No	Command	Hex	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Parameter
14	GAMSET4N2	9Ah	0	1	↑	1	0	0	1	1	0	1	0	Gamma Set 4bpp Negative 2	9A
			1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40		19
			1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50		1A
			1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60		1C
			1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70		1D
15	GAMSET4N3	9Bh	0	1	↑	1	0	0	1	1	0	1	1	Gamma Set 4bpp Negative 3	9B
			1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80		1E
			1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90		20
			1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0		22
			1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0		24
16	GAMSET4N4	9Ch	0	1	↑	1	0	0	1	1	1	0	0	Gamma Set 4bpp Negative 4	9C
			1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0		26
			1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0		29
			1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0		2F
			1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0		3F
17	SLPOUT	12h	0	1	↑	0	0	0	1	0	0	1	0	Sleep Out	12
			1	1	↑	1	0	1	0	0	1	0	1		A5
18	MADCTL	24h	0	1	↑	0	0	1	0	0	1	0	0	Memory Address Control	24
			1	1	↑	0	0	0	0	0	MV	MY	MX		01
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
19	GATESET	66h	0	1	↑	0	1	1	0	0	1	1	0	Gate Set	66
			1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0		01
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
20	BPPSEL	22h	0	1	↑	0	0	1	0	0	0	1	0	BPP Select	22
			1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0		02
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	1	0	1	0	0	1	0	1		A5
21	DISON	15h	0	1	↑	0	0	0	1	0	1	0	1	Display On	15
			1	1	↑	1	0	1	0	0	1	0	1		A5
22	WRRAM	2Ch	0	1	↑	0	0	1	0	1	1	0	0	Write RAM	2C
			1	1	↑	1	0	1	0	0	1	0	1		A5
			1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		

(1)NOP(00H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	1	↑	0	0	0	0	0	0	0	0	00
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Non-operation: This command does not affect any operation.											

(2)SWRESET(AEH)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	1	↑	1	0	1	0	1	1	1	0	AE
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ This command make a reset as same as hardware reset. ▪ It is required Hardware reset at power-on reset. ▪ It is always required to input this command after hardware reset.											

(3)VCMDAT(54H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCMDAT	0	1	↑	0	1	0	1	0	1	0	0	54
1st parameter	1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	0E
2nd parameter	1	1	↑	0	VcomD16	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00
3rd parameter	1	1	↑	0	VcomD26	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	00
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

VcomS[3:0]	VCOM offset data select
0xxx	No offset adjustment
1x00	Parameter 2 of this command(VCOM offset data1)
1x01	Parameter 3 of this command(VCOM offset data2)
1110	External MTP VCOM offser
1111	External MTP VCOM offser
else	TDB

VcomD[6:0] and VcomD2[6:0]	Offset
1000000	-64
1000001	-63
1000010	-62
:	:
1111111	-1
0000000	0
0000001	+1
:	:
0111110	+62
0111111	+63

(4)PWRCTL(61H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTL	0	1	↑	0	1	1	0	0	0	0	1	61
1st parameter	1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	ST3ON	BST2ON	BST1ON	8F
2nd parameter	1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	04
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

- Booster circuit control, source amp setting and booster clock frequency settings.
- This command must be input before SLPOUT command.
- BST3SR[1:0]: Step-up Rate of the 3rd booster setting

  00, 01:"-1"

  10: "-2"

  11: "-3"
- BST4ON ~ BST1ON: 4th ~ 1st booster On/Off setting

  0: Booster off

  1: Booster on
- FOFNo[3:0]: Force off frame, set waiting time by number of frames from sleep out to display on.

(5)EVSET1(62H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EVSET1	0	1	↑	0	1	1	0	0	0	1	0	62
1st parameter	1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	14
2nd parameter	1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	0B
3rd parameter	1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0B
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

- Set each output voltages of built-in voltage regulators.
- VGL = BST3SR[1 : 0] × VGLREG – 3V
- VGH = 2 × VGHREG – VGL
- The voltage of VGL must be lower than AVCLO.

VCOM[6:0]	VCOM(V)
00h	-0.3000
01h	-0.3125
02h	-0.3250
03h	-0.3375
:	:
3Dh	-1.0625
3Eh	-1.0750
3Fh	-1.0875
:	:
7Dh	-1.8625
7Eh	-1.8750
7Fh	-1.8875

VCOM[5:0]	VGHREG(V)
00h	0
01h	1.5
02h	1.6
03h	1.7
:	:
2Eh	6.0
2Fh	6.1
30h	6.2
31h	6.2
:	:
3Eh	6.2
3Fh	6.2

VCOM[4:0]	VCOM(V)
00h	2.4
01h	2.5
02h	2.6
03h	2.7
:	:
1Dh	5.3
1Eh	5.4
1Fh	5.5

(6)DISSET2(33H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISSET2	0	1	↑	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	07
2nd parameter	1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	2F
3rd parameter	1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	10
4th parameter	1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	25
Description	▪ Set source and gate ON/OFF timing ▪ SOnT: Set source on timing by "number of clock from start – 1" ▪ SOffT: Set source off timing by "number of clock from start – 1" ▪ GOnT: Set gate on timing by "number of clock from start – 1" ▪ GOffT: Set gate off timing by "number of clock from start – 1" ▪ HClkNo > SOffT > GOffT											

(7)EVSET2(63H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EVSET2	0	1	↑	0	1	1	0	0	0	1	1	63
1st parameter	1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0E
2nd parameter	1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0E
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

GVDD[4:0]	GVDD(V)
00h	3.1
01h	3.2
02h	3.3
03h	3.4
:	:
1Dh	6.0
1Eh	6.1
1Fh	6.2

GVCL[4:0]	GVDD(V)
00h	-3.1
01h	-3.2
02h	-3.3
03h	-3.4
:	:
1Dh	-6.0
1Eh	-6.1
1Fh	-6.2

(8)DISSET1(32H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISSET1	0	1	↑	0	0	1	1	0	0	1	0	32
1st parameter	1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	32
2nd parameter	1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0	2A
3rd parameter	1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	80
4th parameter	1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	2A

Description

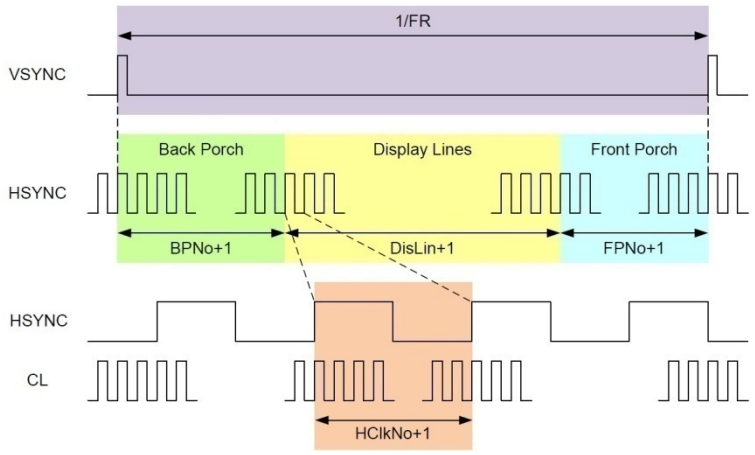
- Set display conditions
- HClkNo = number of clocks in 1H − 1
- BPNo = number of back porch − 1
- FPNo = number of front porch − 1
- NorBlk: Select LCD type

  0: Normally black

  1: Normally white
- OSCO: OSCO pin function

  0: VSS output

  1: Clock output
- Frame rate $= \dfrac{10^6}{(BPNo+DisLin+FPNo+3)\,(HClkNo+1)}$ (Hz)



(9)GAMSET4P1(91H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P1	0	1	↑	1	0	0	1	0	0	0	1	91
1st parameter	1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00
2nd parameter	1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	13
3rd parameter	1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	16
4th parameter	1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	18
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV0: V0 voltage setting (positive polarity) ▪ G4BPV1: V1 voltage setting (positive polarity) ▪ G4BPV2: V2 voltage setting (positive polarity) ▪ G4BPV3: V3 voltage setting (positive polarity)											

(10)GAMSET4P2(92H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P2	0	1	↑	1	0	0	1	0	0	1	0	92
1st parameter	1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	19
2nd parameter	1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	1A
3rd parameter	1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	1B
4th parameter	1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1D
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV4: V4 voltage setting (positive polarity) ▪ G4BPV5: V5 voltage setting (positive polarity) ▪ G4BPV6: V6 voltage setting (positive polarity) ▪ G4BPV7: V7 voltage setting (positive polarity)											

(11)GAMSET4P3(93H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P3	0	1	↑	1	0	0	1	0	0	1	1	93
1st parameter	1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	1F
2nd parameter	1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	20
3rd parameter	1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	22
4th parameter	1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	24
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV8: V8 voltage setting (positive polarity) ▪ G4BPV9: V9 voltage setting (positive polarity) ▪ G4BPV10: V10 voltage setting (positive polarity) ▪ G4BPV11: V11 voltage setting (positive polarity)											

(12)GAMSET4P4(94H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P4	0	1	↑	1	0	0	1	0	1	0	0	94
1st parameter	1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	26
2nd parameter	1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	29
3rd parameter	1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	2F
4th parameter	1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV12: V12 voltage setting (positive polarity) ▪ G4BPV13: V13 voltage setting (positive polarity) ▪ G4BPV14: V14 voltage setting (positive polarity) ▪ G4BPV15: V15 voltage setting (positive polarity)											

(13)GAMSET4N1(99H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N1	0	1	↑	1	0	0	1	1	0	0	1	99
1st parameter	1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00
2nd parameter	1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	13
3rd parameter	1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	15
4th parameter	1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	17
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNV0: V0 voltage setting (negative polarity) ▪ G4BNV1: V1 voltage setting (negative polarity) ▪ G4BNV2: V2 voltage setting (negative polarity) ▪ G4BNV3: V3 voltage setting (negative polarity)											

(14)GAMSET4N2(9AH)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N2	0	1	↑	1	0	0	1	1	0	1	0	9A
1st parameter	1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	19
2nd parameter	1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	1A
3rd parameter	1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	1C
4th parameter	1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1D
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNV4: V4 voltage setting (negative polarity) ▪ G4BNV5: V5 voltage setting (negative polarity) ▪ G4BNV6: V6 voltage setting (negative polarity) ▪ G4BNV7: V7 voltage setting (negative polarity)											

(15)GAMSET4N3(9BH)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N3	0	1	↑	1	0	0	1	1	0	1	1	9B
1st parameter	1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	1E
2nd parameter	1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	20
3rd parameter	1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	22
4th parameter	1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	24
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNV8: V8 voltage setting (negative polarity) ▪ G4BNV9: V9 voltage setting (negative polarity) ▪ G4BNVA: V10 voltage setting (negative polarity) ▪ G4BNVB: V11 voltage setting (negative polarity)											

(16)GAMSET4N4(9CH)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N4	0	1	↑	1	0	0	1	1	1	0	0	9C
1st parameter	1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	26
2nd parameter	1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	29
3rd parameter	1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	2F
4th parameter	1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNVC: V12 voltage setting (negative polarity) ▪ G4BNVD: V13 voltage setting (negative polarity) ▪ G4BNVE: V14 voltage setting (negative polarity) ▪ G4BNVF: V15 voltage setting (negative polarity)											

(17)SLPOUT(12H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	1	↑	0	0	0	1	0	0	1	0	12
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ It is required hardware reset at power-on. ▪ It is always required to input this command after hardware reset.											

(18)MADCTL(24H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	1	↑	0	0	1	0	0	1	0	0	24
1st parameter	1	1	↑	0	0	0	0	0	MV	MY	MX	1
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set about display data RAM. ▪ To access display RAM, it is required 1ms or more wait after input this command. ▪ MV: Select address incremental direction.(refer to 6.2.3) 0: Incremental column addr. 1: Incremental page addr. ▪ MY: Display data RAM page address (refer to 6.2.3) 0: Normal 1: Reverse ▪ MX: Display data RAM column address (refer to 6.2.3) 0: Normal 1: Reverse											

(19)GATESET(66H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATESET	0	1	↑	0	1	1	0	0	1	1	0	66
1st parameter	1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	01
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set line scan mode of gate driver. ▪ This command must be input before SLPOUT command. ▪ VGPP: Valid gate pin postion 0: Inside 1: Outside ▪ ScanDir: Scan direction 0: Normal 1: Reverse ▪ ScanMode[1:0]: Scan mode (refer to 6.4) 00: scan mode 1 01: scan mode 2 10: scan mode 3 11: scan mode 4											

(20)BPPSEL(22H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPPSEL	0	1	↑	0	0	1	0	0	0	1	0	22
1st parameter	1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0	02
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set data format (bit per pixel) ▪ It is enabled next frame after receiving the command. ▪ It is possible to change 4bpp / 2bpp / 1bpp. ▪ It must be input during display off state, and display data must be written after changing ▪ BppSel[1:0] : Set data format (bit per pixel) 00: 1bpp (2 gray scale) 01: 2bpp (4 gray scale) 10: 4bpp (16 gray scale)											

(21) DISON(15H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISON	0	1	↑	0	0	0	1	0	1	0	1	15
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Start to display. ▪ SLPOUT command must be input before this command. ▪ After SLPOUT command, DISON command is waited until “display possible state” and this command is executed after wait time set by PWRCTL command.											

(22)WRRAM(2CH)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRRAM	0	1	↑	0	0	1	0	1	1	0	0	2C
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Write data	1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	
Description	▪ After this WRRAM command, data is input at display area which is set by CASET and PASET command. ▪ RAM address is incremented automatically by WR signal. ▪ Column address, page address and frame address are set to start addresses by WRRAM command input. ▪ There is no limit to input data, and it is continued to be written until next command input. ▪ When the address arrives to end address, it is return to start address.											

9.3 TIMING CHART

A. DATA TRANSFER.

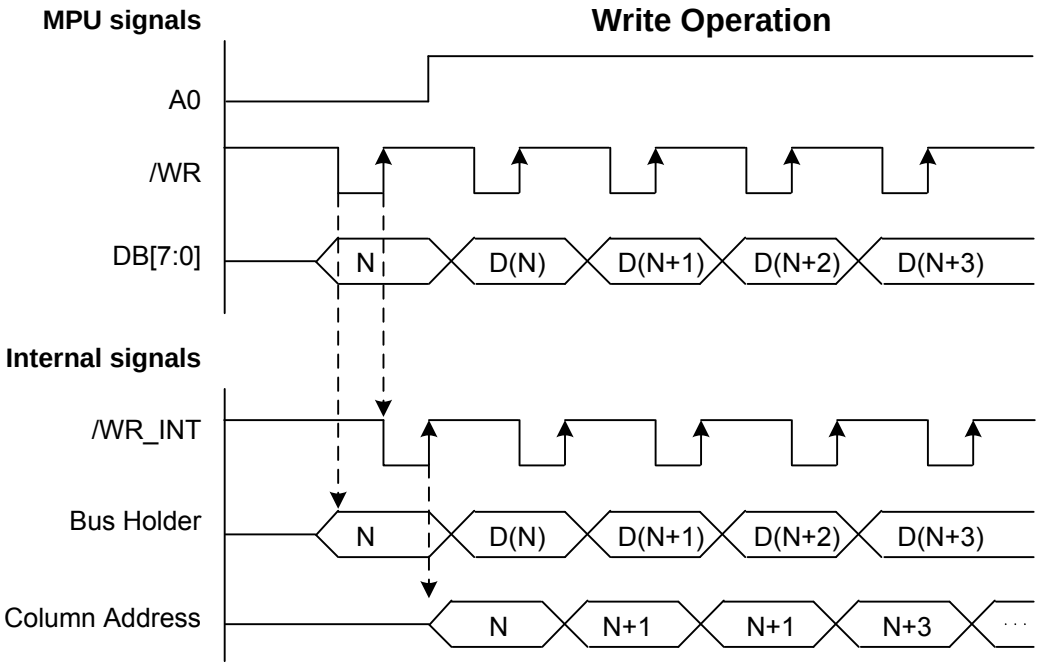


Fig. 9.1 Data transfer: Write

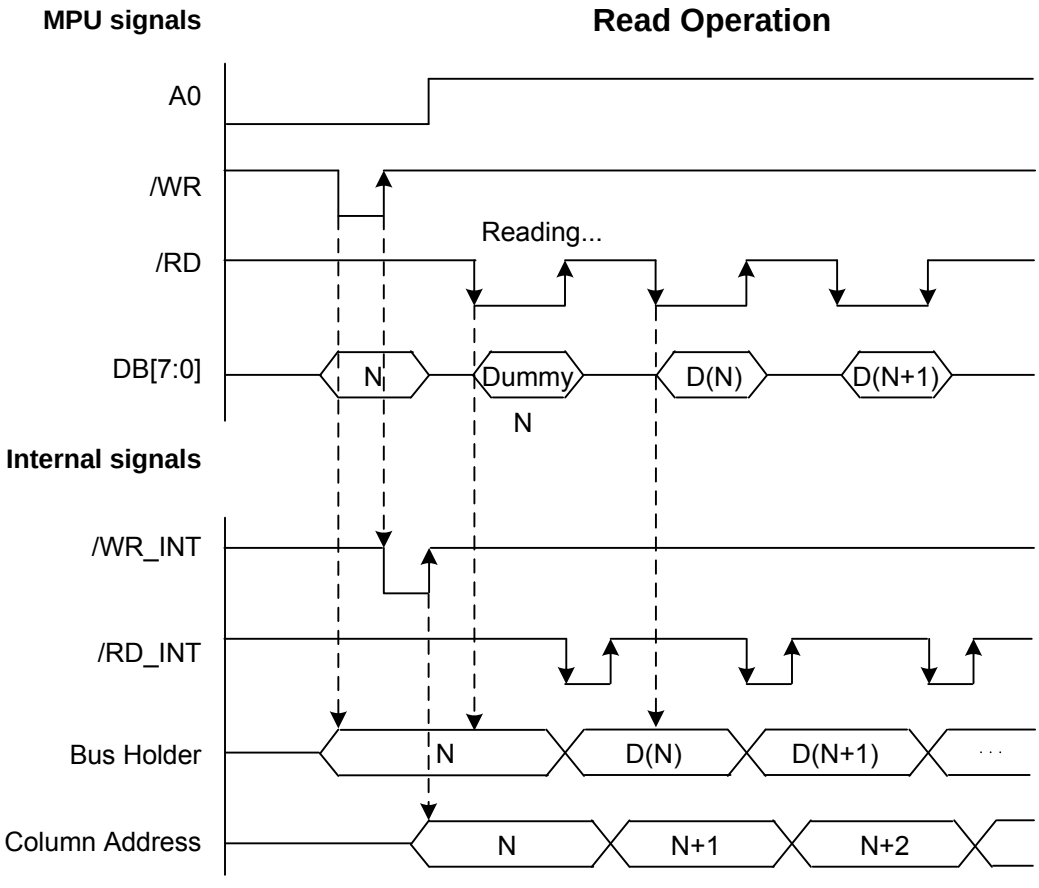


Fig. 9.2 Data transfer: Read

B. SYSTEM BUS TIMING FOR 8080 SERIES MPU

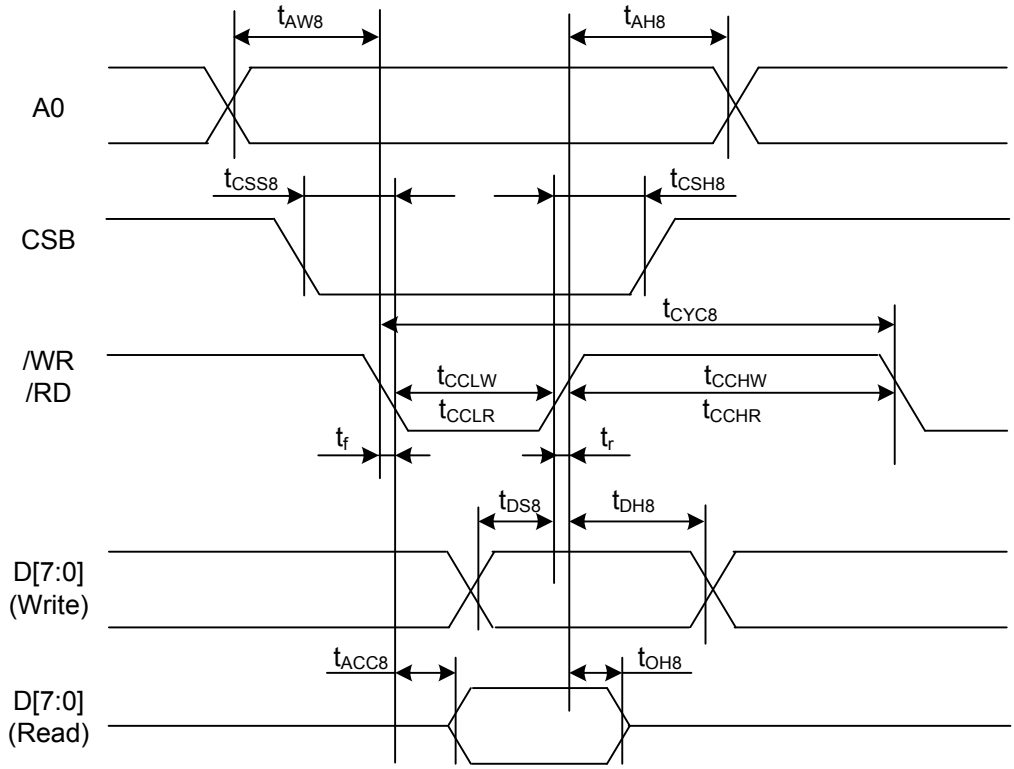


Fig. 9.3 8080 Series MPU Timing

9.4 TIMING TABLE

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance.

A. SYSTEM BUS TIMING FOR 8080 SERIES MPU

Item		Symbol	Condition	Min.	Max.	Unit
A0	Address setup time	tAW8	-	10	-	ns
	Address hold time	tAH8	-	0	-	
/WR	System cycle time	tCYC8	-	200	-	
	WR L Pulse width(WRITE)	tCCLW	-	100	-	
	WR H Pulse width(WRITE)	tCCHW	-	100		
/RD	RD L Pulse width(READ)	tCCLR	-	120	-	
	RD H Pulse width(READ)	tCCHR	-	120	-	
CSB	CSB setup time	tCSS8	-	100	-	
	CSB hold time	tCSH8	-	100	-	
D[7:0]	WRITE Data setup time	tDS8	-	70	-	
	WRITE Data hold time	tDH8	-	20	-	
	READ access time	tACC8	CL = 100PF	-	80	
	READ Output disable time	tOH8	CL = 100PF	15	80	

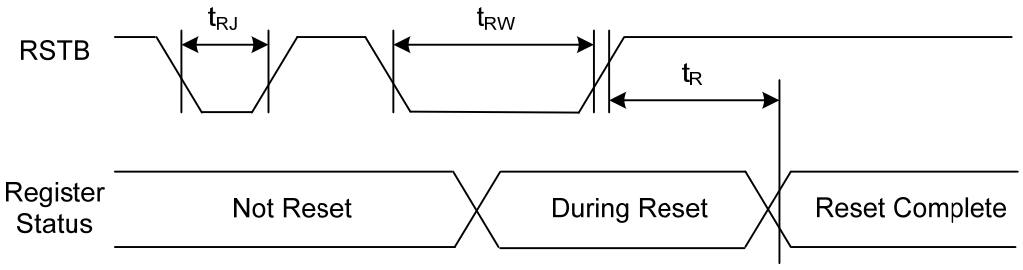
Note 1: The input signal rise time and fall time (tr, tf) is specified at 15ns or less. When the system cycle time is extremely fast.

(tr + tf)≧ (tCYCB – tCCLW – tCCHW) for (tr + tf) ≦(tCYCB – tCCLR – tCCHR) are specified.

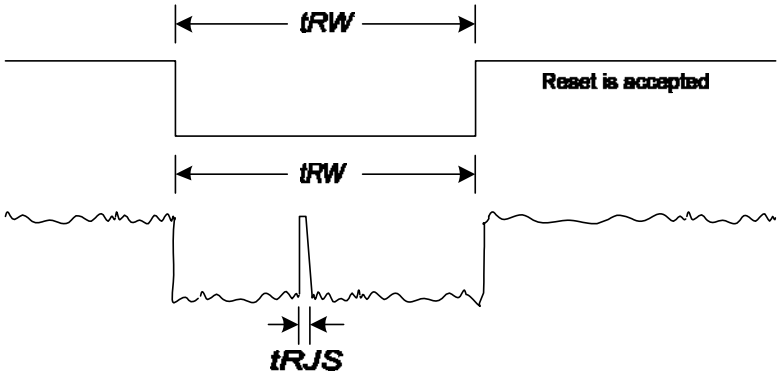
Note 2: All timing is specified using 20% and 80% of VDDI as the reference.

Note 3: tCCLW and tCCLR are specified as the overlap between CS being “L” and WR and RD being at the “L” level. CS and WR (or RD) cannot act at the same time and CS should be 100ns wider than WR (or RD).

9.5 Hardware Reset Timing



Item		Symbol	Min.	Typ.	Max.	Unit
RSTB	Reset time	tR	-	-	5	us
	Reset "L" pulse width	tRW	15	-	-	
	Reset rejection	tRJ	-	-	5	
	Reset rejection(for noise spike)	tRJS	-	-	10	ns



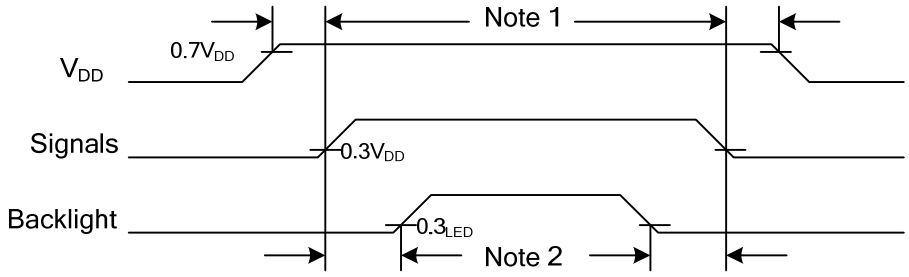
Note 1: For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents.

Do NOT use any PROM related command during this period.

Note 2: When the system issues a RST LOW pulse, the reset procedure of IC will start if the LOW pulse is longer tRW specified above. If the LOW pulse is less than tRJ specified above, the reset procedure of IC will not start.

If the LOW pulse is longer than tRJ and tRW, the procedure of IC is not guaranteed.

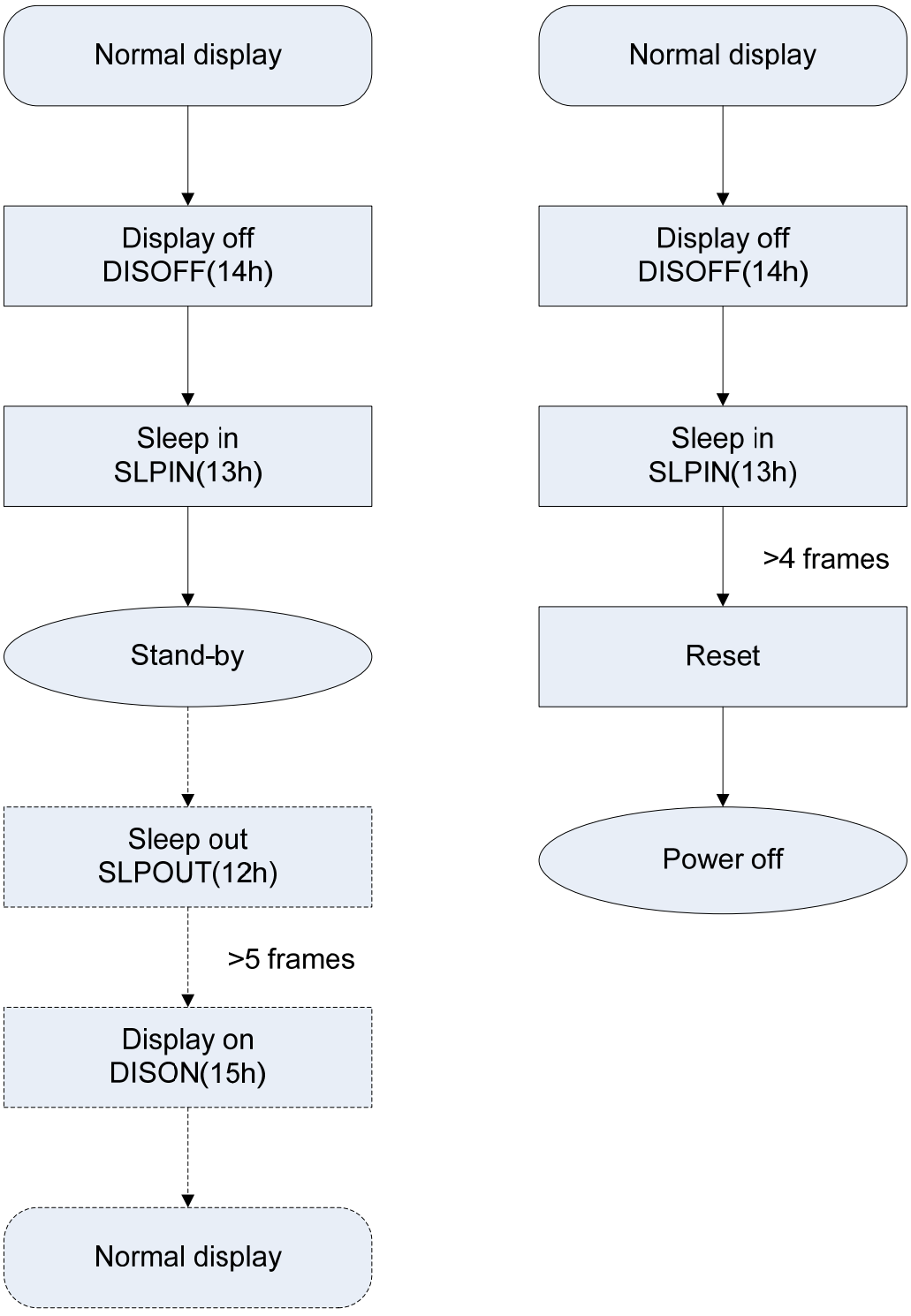
9.6 POWER SEQUENCE



Note 1: In order to avoid any damages, V_{DD} has to be applied before all other signals. The opposite is true for power off where V_{DD} has to be remained on until all other signals have been switch off. The recommended time period is 1 second.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

9.7 STAND-BY AND POWER OFF FLOW



STAND-BY AND POWER OFF Command List

No	Command	Hex	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Parameter
1	DISOFF	14h	0	1	↑	0	0	0	1	0	1	0	0	Display Off	14
			1	1	↑	1	0	1	0	0	1	0	1		A5
2	SLPIN	13h	0	1	↑	0	0	0	1	0	0	1	1	Sleep In	13
			1	1	↑	1	0	1	0	0	1	0	1		A5
3	SLPOUT	12h	0	1	↑	0	0	0	1	0	0	1	0	Sleep Out	12
			1	1	↑	1	0	1	0	0	1	0	1		A5
4	DISON	15h	0	1	↑	0	0	0	1	0	1	0	1	Display On	15
			1	1	↑	1	0	1	0	0	1	0	1		A5

(1) DISOFF(14H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISOFF	0	1	↑	0	0	0	1	0	1	0	0	14
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Display off.											

(2) SLPIN(13H)

Ins./Par.	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	1	↑	0	0	0	1	0	0	1	1	13
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ It is required hardware at power-on reset. ▪ **It is always required to input this command after hardware reset.**											

(3) SLPOUT(12H)

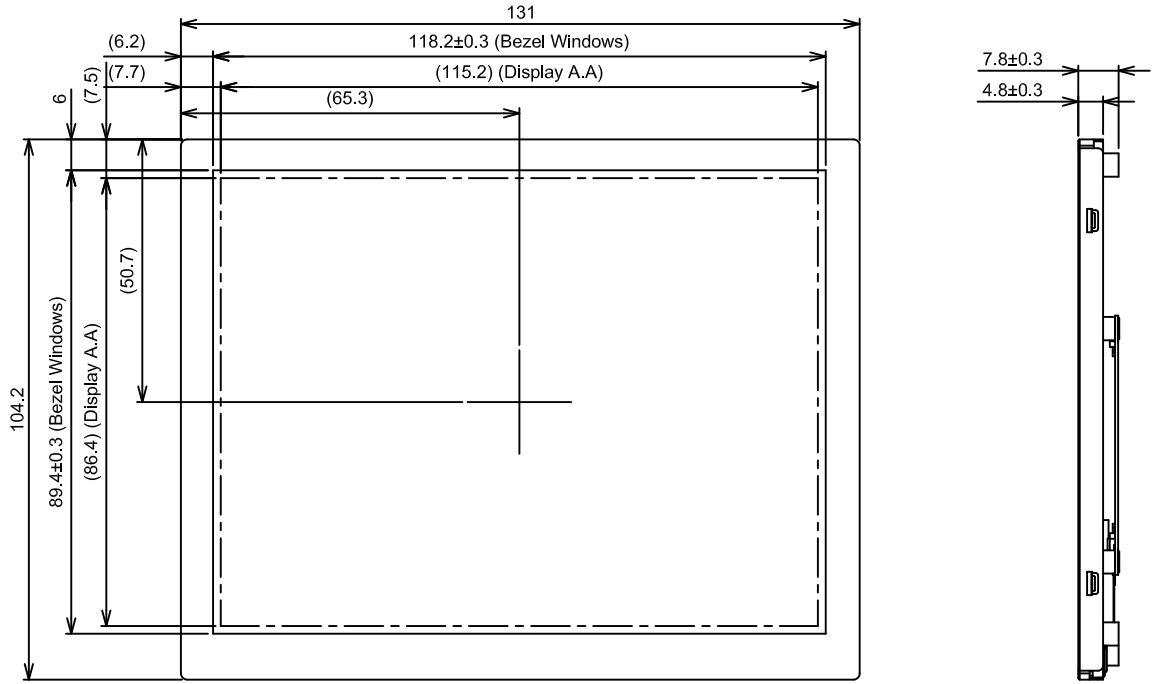
Ins./Par.	A1	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	1	↑	0	0	0	1	0	0	1	0	12
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ It is required hardware reset at power-on. ▪ **It is always required to input this command after hardware reset.**											

(4) DISON(15H)

Ins./Par.	A1	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISON	0	1	↑	0	0	0	1	0	1	0	1	15
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Start to display. ▪ SLPOUT command must be input before this command. ▪ After SLPOUT command, DISON command is waited until “display possible state” and this command is executed after wait time set by PWRCTL command.											

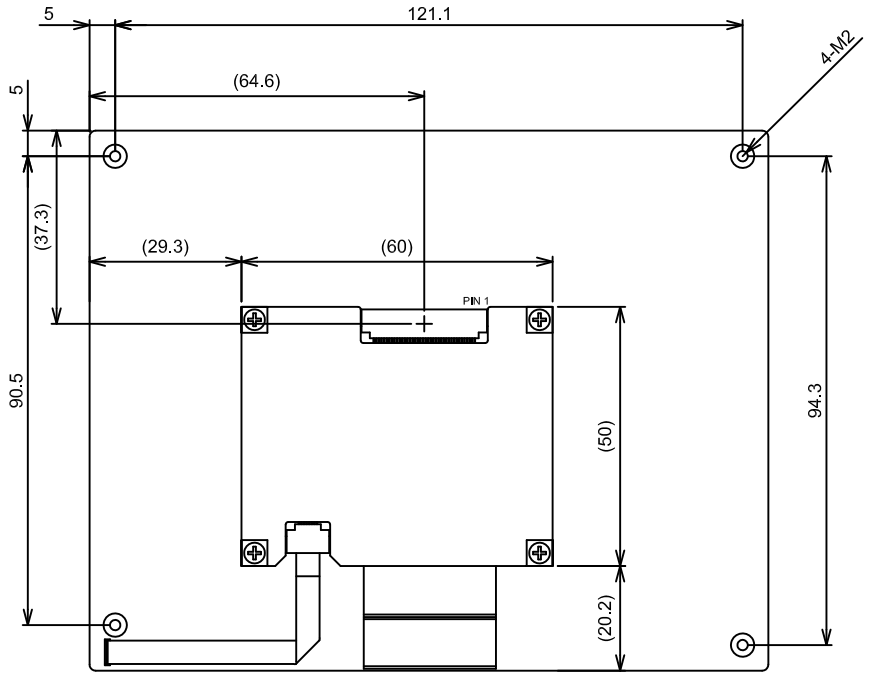
10. OUTLINE DIMENSIONS

10.1 FRONT VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

10.2 REAR VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

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11. APPEARANCE STANDARD

The appearance inspection is performed in a room around 500~1000 lx based on the conditions as below:

- The distance between inspector's eyes and display is 30 cm.
- The viewing zone is defined with angle θ shown in Fig. 11.1 The inspection should be performed within 45° when display is shut down. The inspection should be performed within 5° when display is power on.

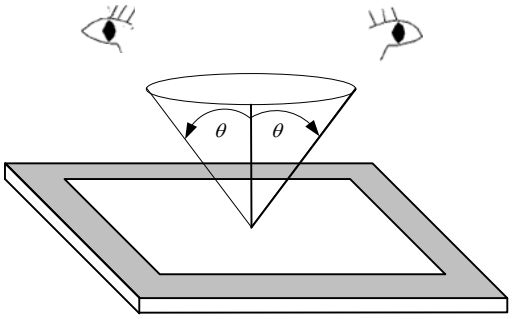


Fig. 11.1

11.1 THE DEFINITION OF LCD ZONE

LCD panel is divided into 2 areas as shown in Fig.11.2 for appearance specification in next section. A zone is the LCD active area (dot area); B zone is the area between A zone and metal frame.

In terms of housing design, B zone is the recommended window area customers' housing should be located in.

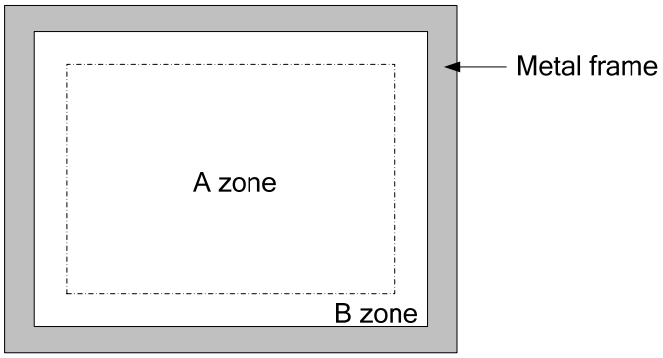


Fig. 11.2

11.2 LCD APPEARANCE SPECIFICATION

The specification as below is defined as the amount of unexpected phenomenon or material in different zones of LCD panel. The definitions of length, width and average diameter using in the table are shown in Fig. 11.4 and Fig. 11.5.

Item	Criteria				Applied zone
Scratches	Length (mm)	Width (mm)	Maximum number	Minimum space	A
	L≦15	W≦0.02	Ignored	-	
	L≦15	0.02＜W≦0.1	5	-	
	L＞15	0.1＜W	0	-	
Wrinkles in polarizer	Serious one is not allowed				A
Bubbles on polarizer / Dent	Average diameter (mm)		Maximum number		A
	D＜0.3		Ignored		
	0.3≦D≦0.6		4		
	0.6＜D		0		
1) Stains 2) Foreign Materials 3) Dark Spot	Filamentous (Line shape)				A
	Length (mm)	Width (mm)	Maximum number		
	L≦2.0	W≦1.5	5		
	L＞2.0	1.5＜W	0		
	Round (Dot shape)				A
	Average diameter (mm)	Maximum number	Minimum Space		
	D＜0.2	Ignored	-		
	0.2≦D≦0.6	4	-		
	0.6＜D	0	-		
	Those wiped out easily are acceptable				
Dot-Defect		Area①	Area②	Maximum number	A (Note 1)
	Bright dot-defect	1 dot	2 dot	3 dot	
	Dark dot-defect	2 dot	3 dot	4 dot	
	Bright + Dark point	3 dot	4 dot	5 dot	

Note 1: The Dot-Defect inspection within A zone (active area) would be divided into area ①, ② as Fig. 11.3 shown.

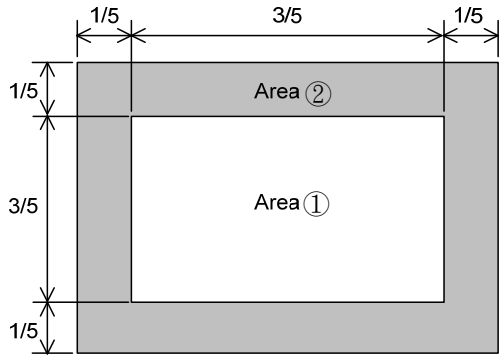


Fig. 11.3

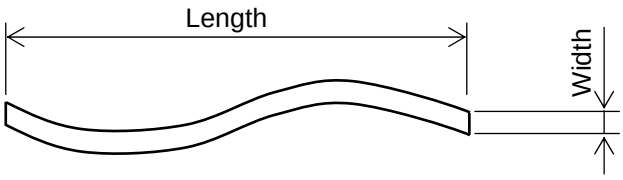
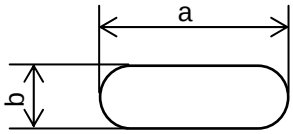


Fig 11.4



Average diameter = $\frac{a+b}{2}$

Fig 11.5

Note 2: The definitions of dot defect are as below:

- The defect area of the dot must be bigger than half of a dot.

12. PRECAUTIONS

12.1 PRECAUTIONS of ESD

1) Before handling the display, please ensure your body has been connected to ground to avoid any damages by ESD. Also, do not touch display's interface directly when assembling.

2) Please remove the protection film very slowly before turning on the display to avoid generating ESD.

12.2 PRECAUTIONS of HANDLING

1) In order to keep the appearance of display in good condition; please do not rub any surfaces of the displays by sharp tools harder than 3H, especially touch panel, metal frame and polarizer.

2) Please do not pile the displays in order to avoid any scars leaving on the display. In order to avoid any injuries, please pay more attention for the edges of glasses and metal frame, and wear finger cots to protect yourself and the display before working on it.

3) Touching the display area or the terminal pins with bare hand is prohibited. This is because it will stain the display area and cause poor insulation between terminal pins, and might affect display's electrical characteristics furthermore.

4) Do not use any harmful chemicals such as acetone, toluene, and isopropyl alcohol to clean display's surfaces.

5) Please use soft cloth or absorbent cotton with ethanol to clean the display by gently wiping. Moreover, when wiping the display, please wipe it by horizontal or vertical direction instead of circling to prevent leaving scars on the display's surface, especially polarizer.

6) Please wipe any unknown liquids immediately such as saliva, water or dew on the display to avoid color fading or any permanently damages.

7) Maximum pressure to the surface of the display must be less than $1{,}96 \times 10^4$ Pa. If the area of adding pressure is less than $1\,cm^2$, the maximum pressure must be less than 1.96N.

12.3 PRECAUTIONS OF OPERATING

1) Please input signals and voltages to the displays according to the values defined in the section of electrical characteristics to obtain the best performance. Any voltages over than absolute maximum rating will cause permanent damages to this display. Also, any timing of the signals out of this specification would cause unexpected performance.

2) When the display is operating at significant low temperature, the response time will be slower than it at $25\,C^\circ$. In high temperature, the color will be slightly dark and blue compared to original pattern. However, these are temperature-related phenomenon of LCD and it will not cause permanent damages to the display when used within the operating temperature.

3) The use of screen saver or sleep mode is recommended when static images are likely for long periods of time. This is to avoid the possibility of image sticking.

4) Spike noise can cause malfunction of the circuit. The recommended limitation of spike noise is no bigger than ± 100 mV.

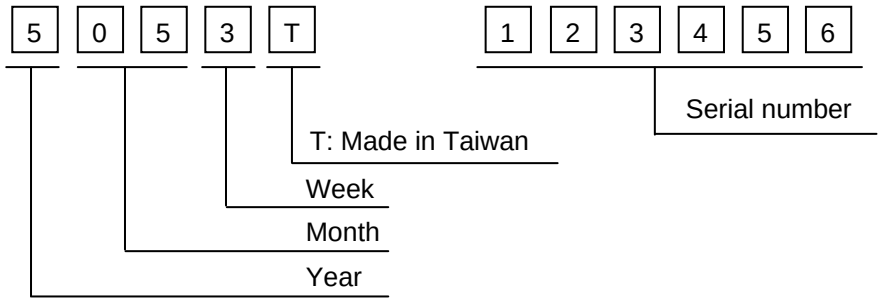
12.4 PRECAUTIONS of STORAGE

If the displays are going to be stored for years, please be aware the following notices.

1) Please store the displays in a dark room to avoid any damages from sunlight and other sources of UV light.
2) The recommended long-term storage temperature is between 10℃~35℃ and 55%~75% humidity to avoid causing bubbles between polarizer and LCD glasses, and polarizer peeling from LCD glasses.
3) It would be better to keep the displays in the container, which is shipped from KOE, and do not unpack it.
4) Please do not stick any labels on the display surface for a long time, especially on the polarizer.

13. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.13.3. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.



2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Mark
2015	5
2016	6
2017	7
2018	8
2019	9

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

Week (Days)	Mark
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5

3) The location of the lot mark is on the back of the display shown in Fig. 13.3.

Fig 13.3